Laboratory 1

(Due date: **002**: January 20th, **003**: January 20th, **004**: January 21st)

OBJECTIVES

- ✓ Introduce VHDL Coding for FPGAs.
- ✓ Learn to write testbenches in VHDL.
- ✓ Learn the Xilinx FPGA Design Flow with the ISE 14.7 Webpack: Synthesis, Simulation, and Bitstream Generation.
- ✓ Learn how to assign FPGA I/O pins and download the bitstream on the Nexys™-4 Artix-7 FPGA Board.

VHDL CODING

- ✓ Refer to the Tutorial: VHDL for FPGAs for a list of examples.

NEXYS™-4 ARTIX-7 FPGA BOARD SETUP

- The Nexys-4 Board can receive power from the Digilent USB-JTAG Port (J6). Connect your Board to a computer via the USB cable. If it does not turn on, connect the power supply of the Board.
- Nexys-4 documentation: Available in class website.

FIRST ACTIVITY (100/100)

- **PROBLEM**: A lock is opened (f='1') only for three combinations of switches: `1100`, `0101`, `1101`, where '1' represents the ON position of a switch and '0' the OFF position.

  - ✓ Complete the truth table for this circuit:

  - ✓ Simplify the Boolean expression:

    $f =$

A	B	C	D	F
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

- **XILINX FPGA DESIGN FLOW**:
  - ✓ Create a new ISE Project. Select the **XC7A100T-3CSG24 Artix-7 FPGA** device.
  - ✓ Write the VHDL code that implements the simplified Boolean expression. Synthesize your circuit (Synthesize – XST)
  - ✓ Write the VHDL testbench to test the circuit for every possible combination of the inputs.
  - ✓ Perform Functional Simulation (Simulate Behavioral Model). **Demonstrate this to your TA.**
  - ✓ I/O Assignment: Create the UCF file. Use SW0 to SW3 on the Nexys-4 Board for the inputs, and LED(0) for the output
  - ✓ Implement your design (Implement Design).
  - ✓ Perform Timing Simulation (Simulate Post-Place & Route Model). **Demonstrate this to your TA.**
  - ✓ Generate the bitstream file (Generate Programming File).
  - ✓ Download the bitstream on the FPGA (Configure Target Device) and test. **Demonstrate this to your TA.**

- Submit (as a .zip file) the generated files: VHDL code, VHDL testbench, and UCF file to Moodle (an assignment will be created). DO NOT submit the whole ISE Project.

TA signature: _____ **Date:** _____

Instructor: Daniel Llamocca
TAs: Bryant Jones, Michael Lohrer, Azam Tayyebi